REMARKS

Claims 1-32 are pending in the present application.

This Amendment is in response to the Office Action mailed September 17, 2002. In the Office Action, the Examiner objected to the drawings, rejected claims 1-2, 14-15, and 27-28 under 35 U.S.C. §102(e); and claims 3-13, 16-26, and 29-32 under 35 U.S.C. §103(a). Applicant has amended claims 1, 14, and 27. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

I. DRAWINGS

In the Office Action, the drawings were objected to in light of cited informalities. In response, Applicant has amended Figure 2 in which the proposed changes are made in red ink. A separate letter regarding these proposed changes is being sent to the draftsperson as set forth in MPEP 602.02(r). Applicant respectfully requests acceptance of the amended Figure because no substantive new matter has been added. Applicant respectfully requests postponement in submitting the formal drawings until the pending claims have been allowed.

II. REJECTIONS UNDER 35 U.S.C. §102(e) AND §103(a)

In the Office Action, the Examiner rejected claims 1-2, 14-15, and 27-28 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,237,064 B1 issued to Kumar et al. ("Kumar") and claims 3-13, 16-26, and 29-32 under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of U.S. Patent No. 6,438,657 B1 issued to Gilda ("Gilda").

Kumar discloses cache memory with reduced latency by paralleling various memory accesses initiated by the execution unit (Kumar, col. 3, lines 42-44). A first cache, a second cache, and a tag array of a third cache are resident in the processor core (Kumar, col. 3, lines 9-13).

Gilda discloses pipelined snooping of multiple L1 cache lines. A L2 cache control unit provides the processor with access to a private L2 cache (Gilda, col. 11, lines 55-61).

Kumar and Gilda, taken alone or in combination, does not disclose, suggest, or render obvious a chipset cache controller internal to a processor and controlling a chipset cache in a chipset external to the processor.

Claims 1, 14, and 27 have been amended to clarify the claim language.

Therefore, Applicant believes that independent claims 1, 14, and 27 and their respective dependent claims are distinguishable over the cited prior art references.

Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. §102(e) and §103(a) be withdrawn.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

The following is a set of all amended claims.

1. (AMENDED) An apparatus comprising:

a processor cache unit to process a cache access request from a processor core of a processor, the processor cache unit including a processor cache controller and a processor cache; and

a chipset cache controller coupled to the processor cache unit to control a chipset cache located in a chipset internally to the processor in response to the cache access request from the processor core, the chipset being external and coupled to the processor via a bus.

14. (AMENDED) A method comprising:

processing a cache access request from a processor core of a processor by a processor cache unit, the processor cache unit including a processor cache controller and a processor cache; and

controlling a chipset cache located in a chipset internally to the processor in response to the cache access request from the processor core, the chipset being external and coupled to the processor via a bus.

27. (AMENDED) A system comprising:

a memory to store data;

a chipset coupled to memory having a chipset cache; and

a processor coupled to the memory and the chipset via a bus, the processor including a processor core and a cache unit, the cache unit comprising:

a processor cache unit to process a cache access request from the processor core, the processor cache unit including a processor cache controller and a processor cache, and

a chipset cache controller coupled to the processor cache unit to control the chipset cache internally to the processor in response to the cache access request from the processor core.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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Dated: December 17, 2002

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: December 17, 2002.

Tu Nguyen